中国科学院计算技术研究所 INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES

北京开源芯片研究院 BEIJING INSTITUTE OF OPEN SOURCE CHIP

中国开放指令生态（RISC-V）联盟 China RISC-V Alliance

XiangShan: An Open-Source High-Performance RISC-V Processor and Infrastructure for Architecture Research

The XiangShan Team

Institute of Computing Technology (ICT)

Chinese Academy of Sciences (CAS)

ASPLOS'23@Vancouver, Canada

March 25, 2023

Schedule

Time	Topic
9:00-9:25	Introduction of the XiangShan Project
9:25-9:35	***Tutorial Overview and Highlights***
9:35-10:20	Microarchitecture Design and Implementation
	Coffee Break
10:40-12:00	Hands-on Development

What we will cover in this tutorial

- **Highlights XiangShan on Chips, FPGAs, and FireSim**

- **CPU Microarchitecture (45 minutes)**
  - *Design and implementation – How to implement novel ideas on XiangShan*
  - Frontend: branch prediction and instruction fetch
  - Backend: out-of-order scheduler, execution units
  - Load/Store Unit: LSQ, pipelines, TLBs, data caches
  - L2/L3 caches and prefetchers

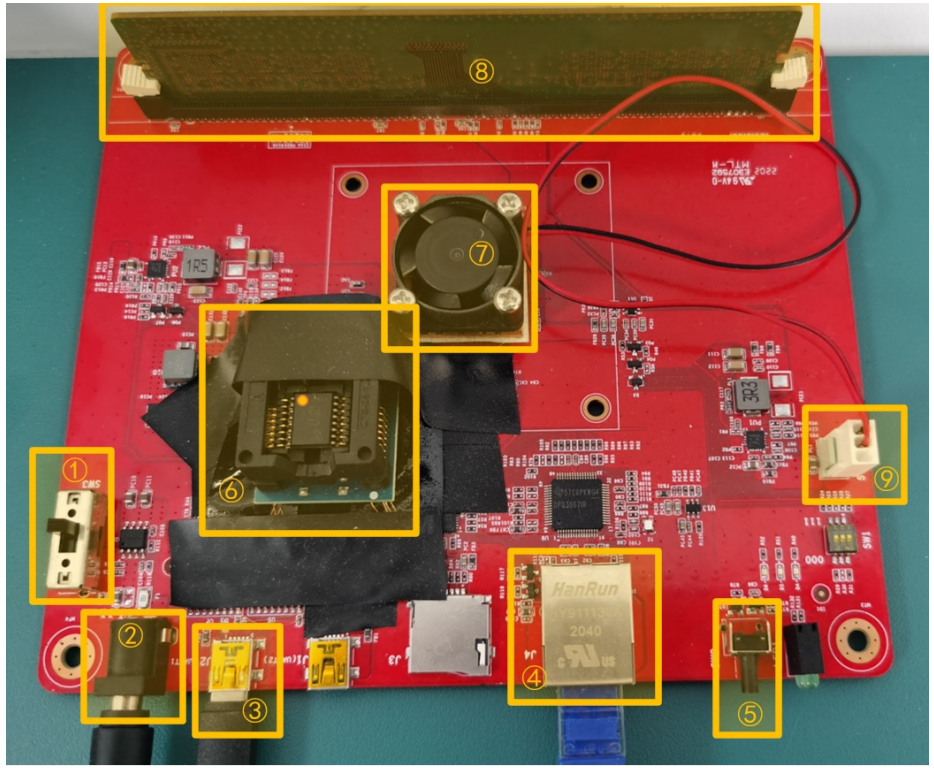
- **Development workflows (80 minutes, 10:40AM after coffee break)**
  - *Introduction of their usages – How to develop XiangShan with MinJie*
  - Simulation and Debugging
  - Research Demo

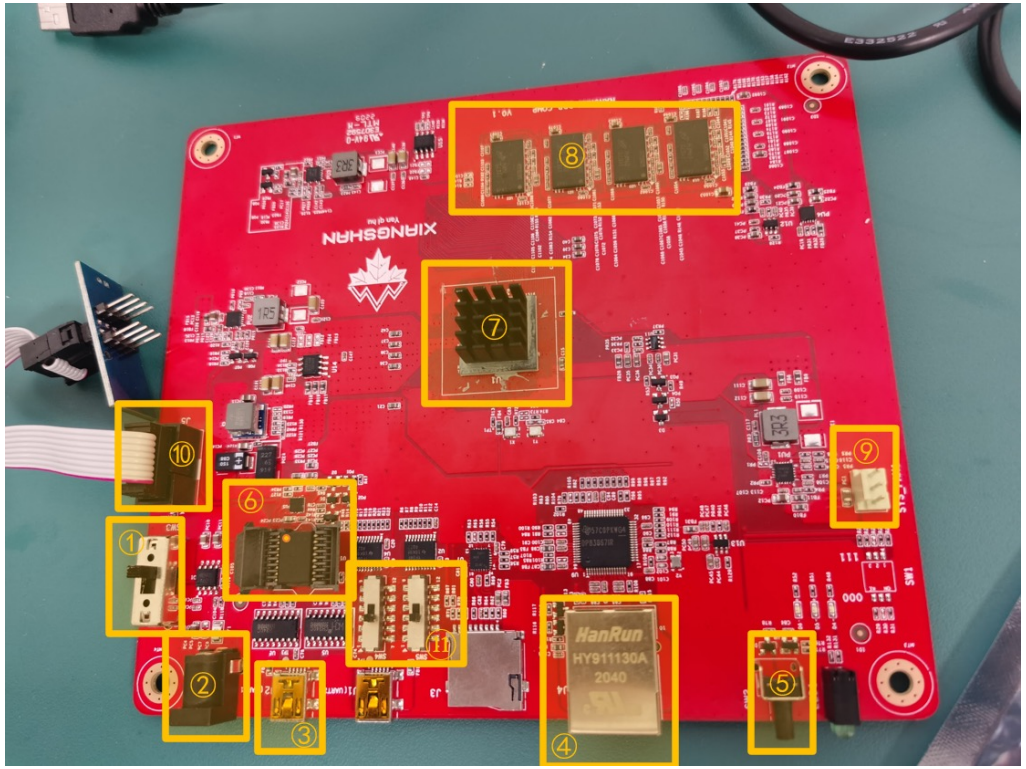
XiangShan: Open-Source at GitHub

- Hardware Designs
  - XiangShan – Main Repo
  - FuDian (FPU)
  - HuanCun (L2/L3)
  - CoupledL2 (next-generation L2)
  - YunSuan (next-generation (V) FPU)
  - Utility
- Software
  - riscv-pk, linux, rootfs
  - GEM5 (partially aligned)
- Dev. Tools
  - Difftest (simulation)
  - NEMU (ISS, ref), Spike (ISS, ref)
  - Nexus-am (bare-metal env)
  - tl-test (L2/L3 unit testing)
  - DRAMsim (forked for co-simulation)
- *We are progressing …*

1st Generation YANQIHU Chips

- Chips run Debian at BOSC and we use SSH to remotely login in

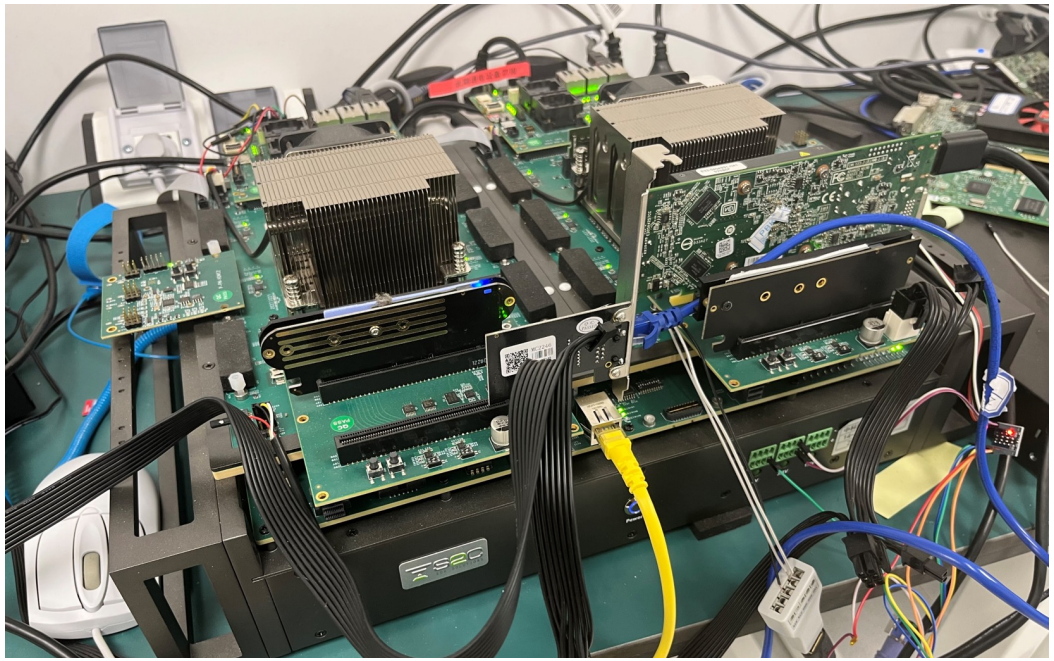


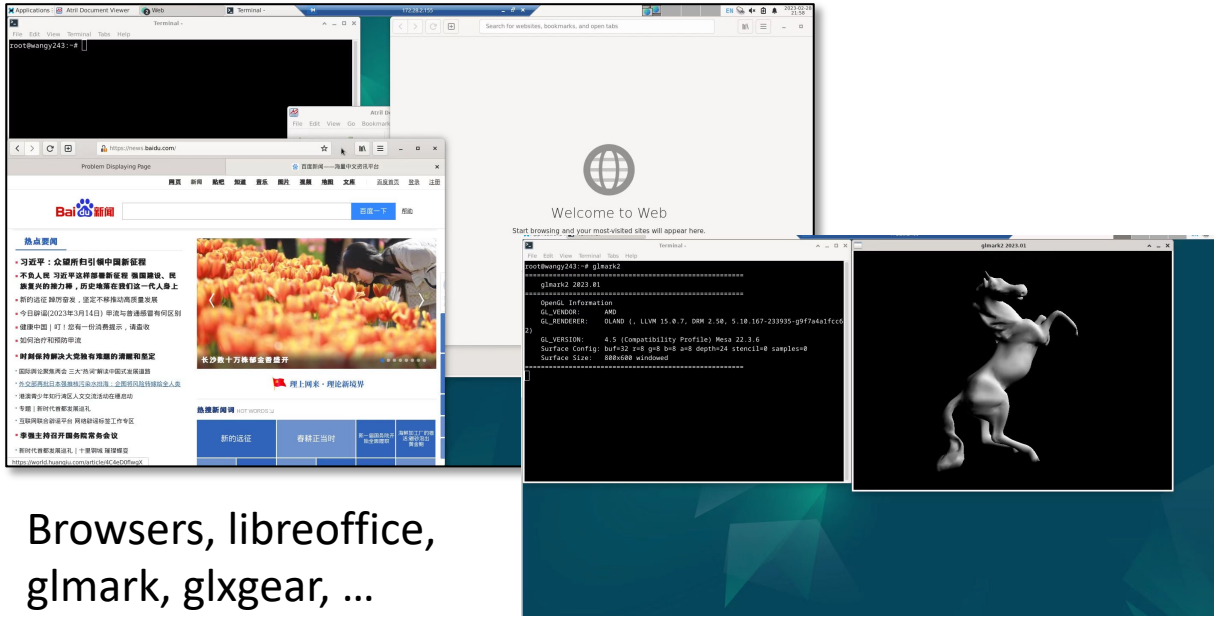


1: switch on/off
2: power
3: serial/UART
4: ethernet
5: reset
6: QSPI flash
7: CPU (with fan)
8: DDR DIMM
9: fan power
10: flash adapter

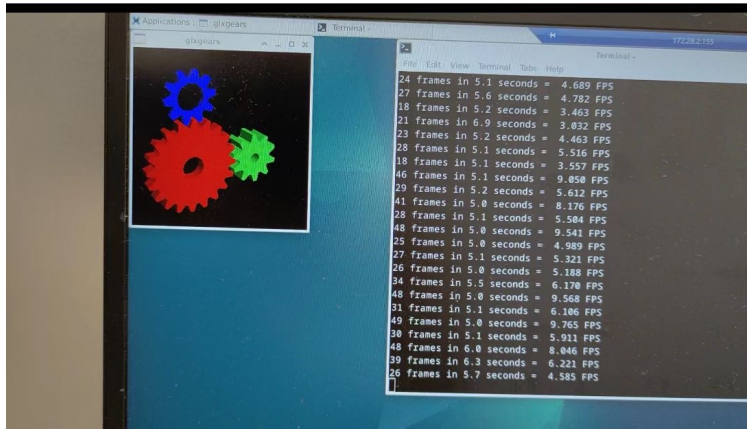
2nd Generation NANHU on FPGA with Graphics

- **Remote desktop access to FPGA at BOSC**





Browsers, libreoffice, glmark, glxgear, …



- Dual-core XiangShan (reduced L3) or normal-size single-core
- S2C Prototyping System with Xilinx VU19P
- No design partition
- UART, Flash, GMAC, PS/2
- NVME/Intel IGB Ethernet/AMD GPU on PCIe

ISE-Enhanced XiangShan on FireSim (done by EPFL)

- **EPFL paper accepted at ISCA'23: Imprecise Store Exceptions (ISE)**
  - Authors: Siddharth Gupta, Yuanlong Li, Qingxuan Kang, Abhishek Bhattacharjee, Babak Falsafi, Yunho Oh, Mathias Payer
- **Simulating Dual-Core MiniConfig XiangShan on *FireSim* (AWS EC2)**

```
INFO: setting up PCIe 0
INFO: loading test.bin...
INFO: done
bbl loader
[    0.000000] Linux version 5.15.0+ (gosh@c006776) (riscv64-linux-gnu-gcc (GCC) 12.2.0,
 GNU ld (GNU Binutils) 2.39) #161 SMP PREEMPT Sat Mar 18 13:51:34 CET 2023
[    0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
[    0.000000] Machine model: freechips,rocketchip-unknown
[    0.000000] earlycon: uartlite_a0 at MMIO 0x0000000040600000 (options '')
[    0.000000] printk: bootconsole [uartlite_a0] enabled
[    0.000000] NUMA: No NUMA configuration found
[    0.000000] NUMA: Faking a node at [mem 0x0000000080200000-0x00000000ffffffff]
[    0.000000] NUMA: NODE_DATA [mem 0xffff6d80-0xffff7fff]
[    0.000000] Zone ranges:
[    0.000000]   DMA32    [mem 0x0000000080200000-0x00000000ffffffff]
[    0.000000]   Normal   empty
[    0.000000] Movable zone start for each node
[    0.000000] Early memory node ranges
[    0.000000]   node   0: [mem 0x0000000080200000-0x00000000ffffffff]
[    0.000000] Initmem setup node 0 [mem 0x0000000080200000-0x00000000ffffffff]
[    0.000000] On node 0, zone DMA32: 512 pages in unavailable ranges
[    0.000000] SBI specification v0.1 detected
[    0.000000] riscv: ISA extensions acdfim
[    0.000000] riscv: ELF capabilities acdfim
```

Linux boot logs on FireSim shared by EPFL

midgard

https://midgard.epfl.ch/

EPFL

More details to be shared at ISCA'23

Thanks!

This tutorial is organized by Kaifan Wang, Yinan Xu, Guokai Chen, Xi Chen, Haoyuan Feng, Ziyue Zhang, Kan Shi, and Yungang Bao.