中国科学院计算技术研究所 INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES

北京开源芯片研究院 BEIJING INSTITUTE OF OPEN SOURCE CHIP

香山开源处理器社区 XiangShan Open-Source Processor Community

DiffTest-H: FPGA 加速 RISC-V 协同仿真 —— 突破 30 MHz 的高性能处理器验证实践

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中国科学院计算技术研究所

2026/10/20@RISC-V 中国峰会，深圳

香山: 性能领先的开源 RISC-V 处理器







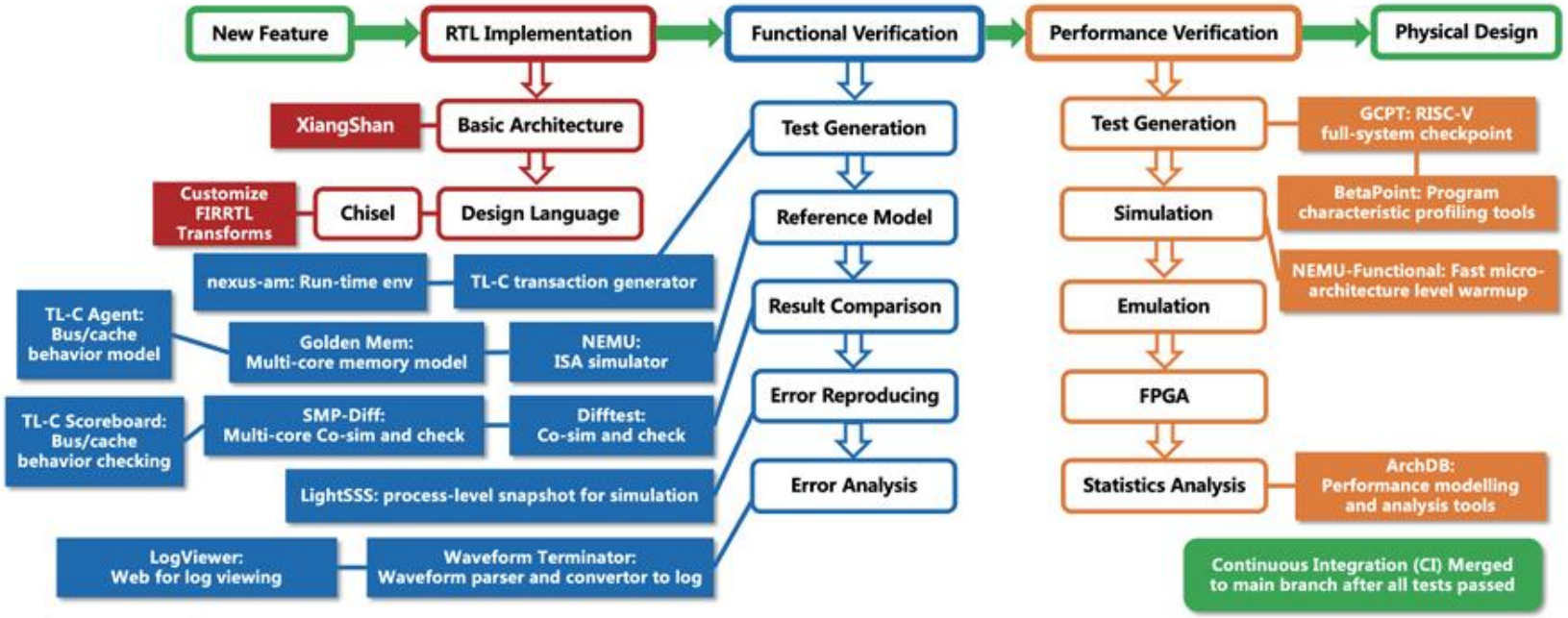




香山: 性能领先的开源 RISC-V 处理器







RISC-V 验证难题：更复杂的指令手册

- **RISC-V ISA 复杂度日益提升**: 指令手册多达数千页

Integer	• Program counter • General-purpose registers • Control and status registers (CSRs)
Double/Float	• Float registers
Vector	• Vector registers • Vector CSRs
Hypervisor	• Hypervisor CSRs
Debug	• Debug CSRs

More than that: Memory Consistency, L1/L2 TLB…

ISA 复杂度: RVA23 Profile

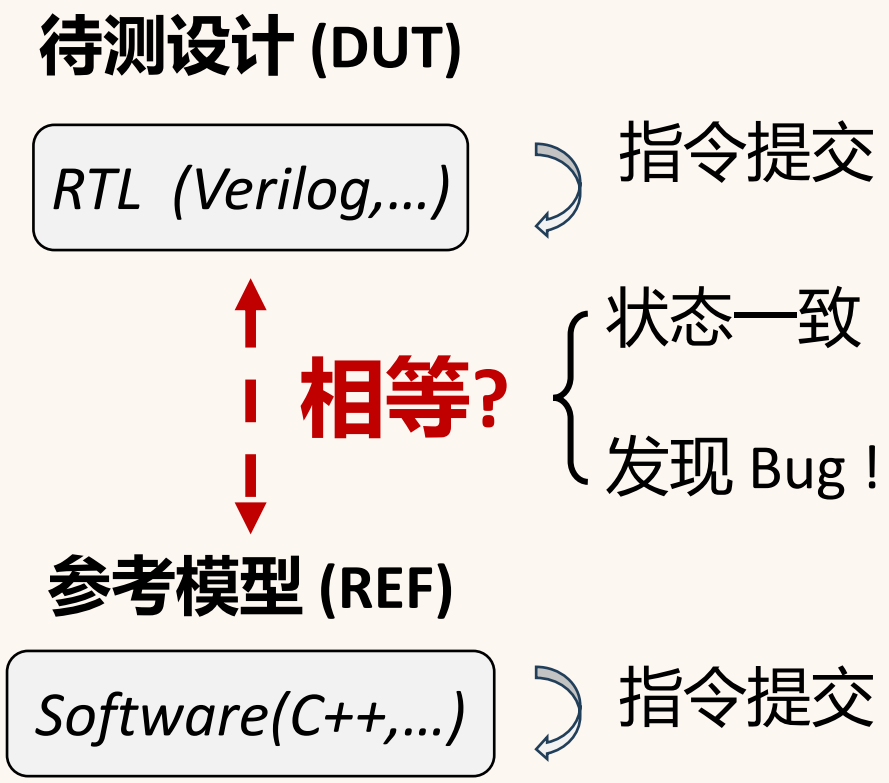
RISC-V 验证难题：需要更充分的验证

- **更充分的验证**：芯片功能正确性的关键保障

Integer	• Program counter • General-purpose registers • Control and status registers (CSRs)
Double/Float	• Float registers
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More than that: Memory Consistency, L1/L2 TLB…

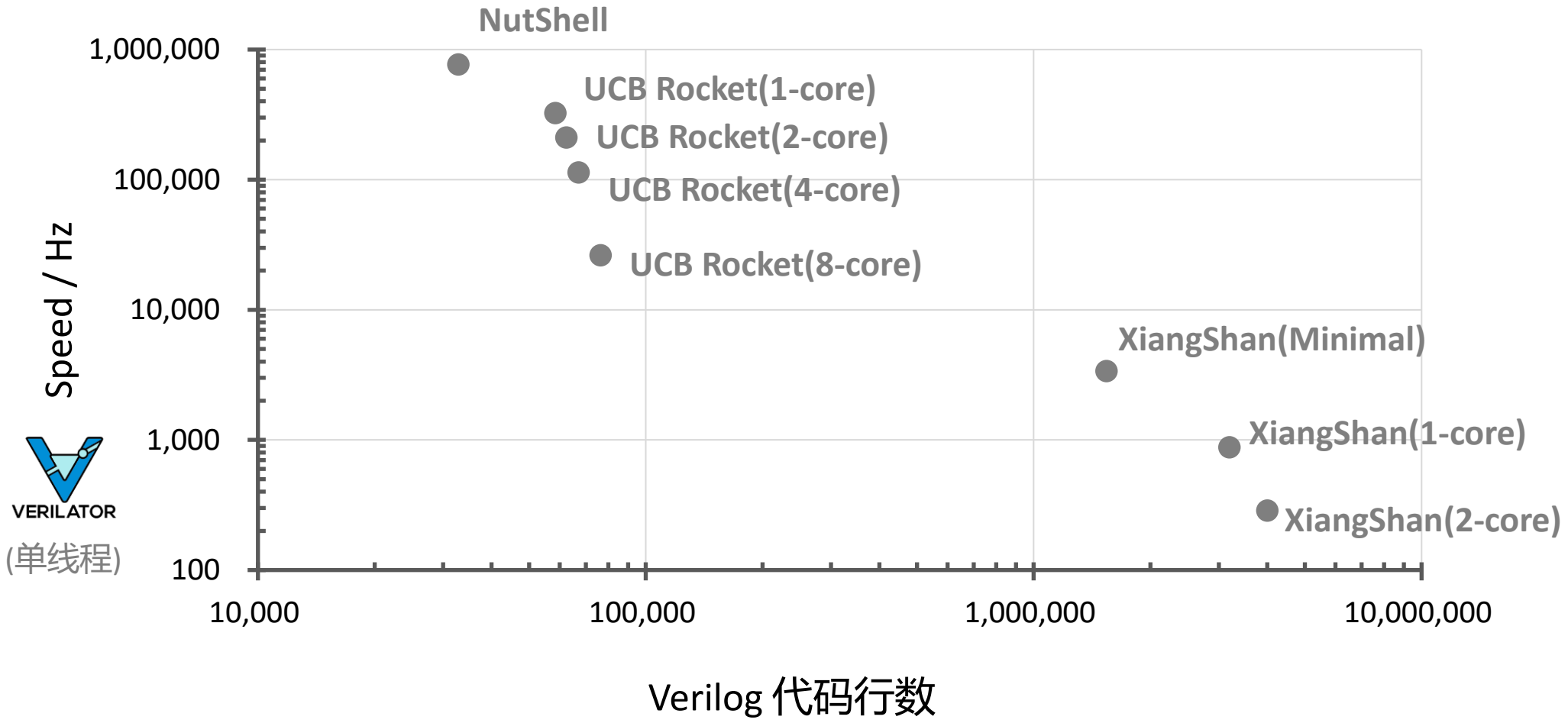
ISA 复杂度: RVA23 Profile



协同仿真: DUT vs. REF

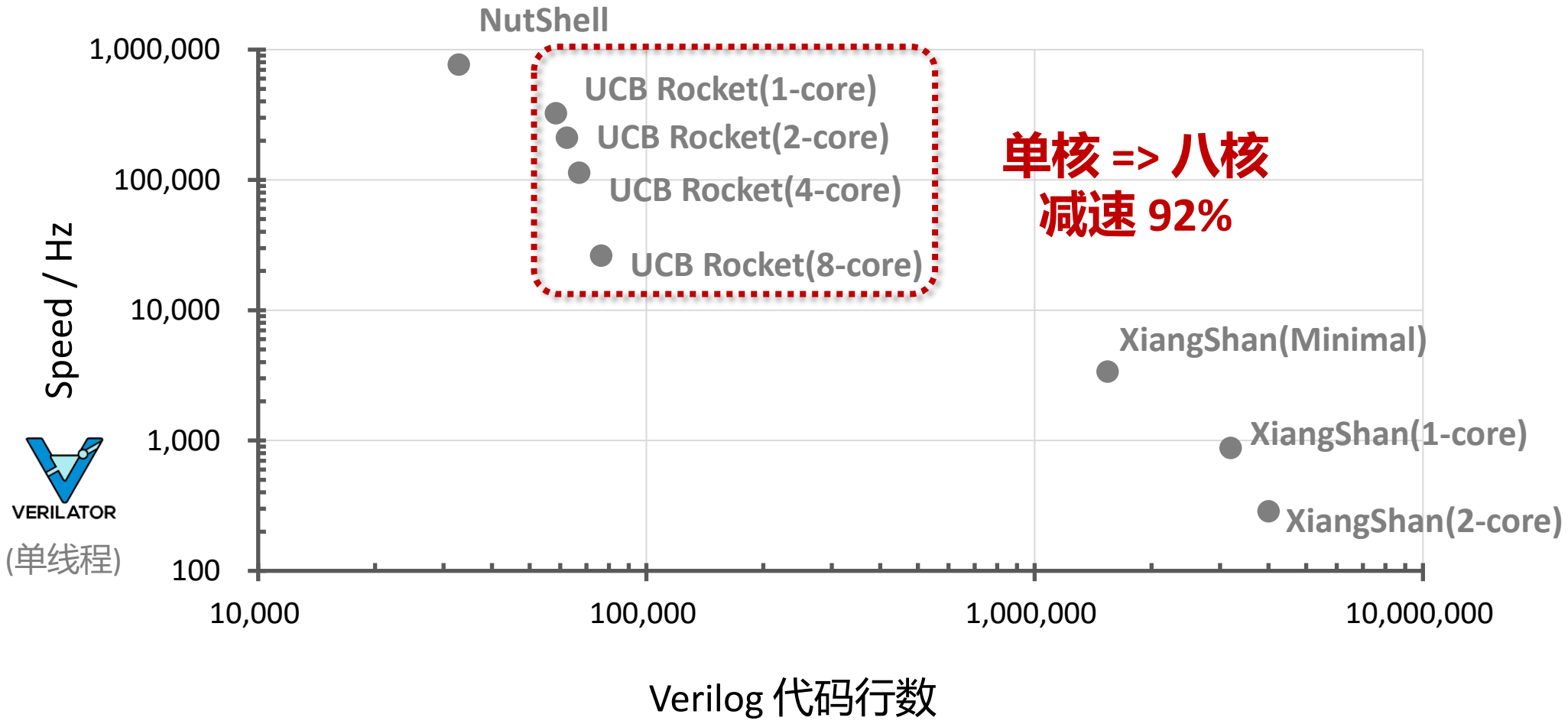
RISC-V 验证难题：仿真速度成为验证瓶颈

- **更充分的验证**：受限**仿真速度**，随规模增大显著减慢



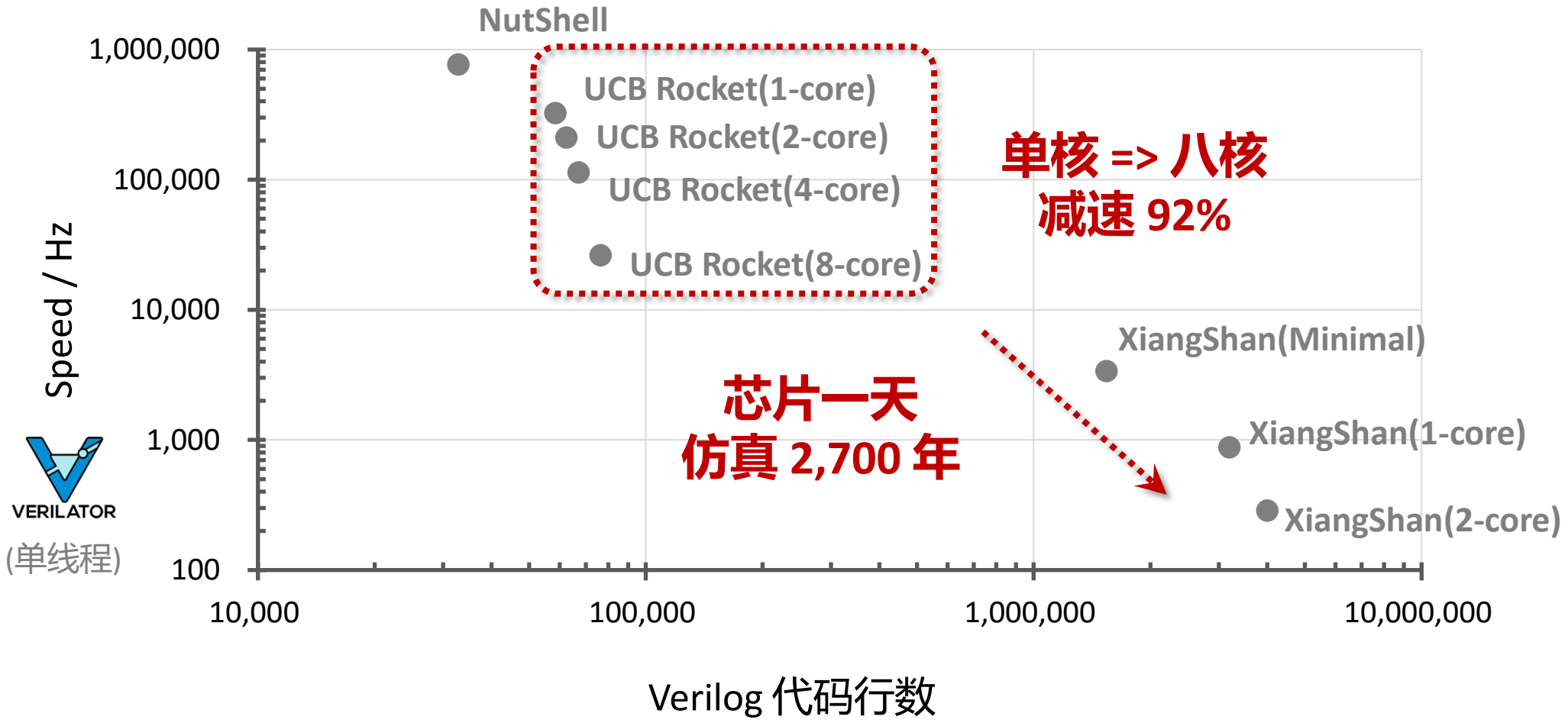
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- **更充分的验证**：受限**仿真速度**，随规模增大显著减慢



RISC-V 验证难题：仿真速度成为验证瓶颈

- **基于软件 RTL 仿真器:** VCS, Verilator, GSIM, …
  - 非常慢（KHz 量级或更低）
  - VCS: 单核香山仿真速度低于 0.1 KHz (cycle/s)
  - Verilator/GSIM: 单核香山仿真速度约 1~3 KHz

- **硬件仿真器**: Cadence Palladium
  - 较快 (MHz 量级), 但价格高达 **数百万美元**

- **FPGAs**: Xilinx VU19P
  - 最快 (数十 MHz), 但缺乏信号可见性，难以定位出错原因

本工作: 快速，易用，调试友好的协同仿真平台



33 MHz@FPGA

RTL 仿真速度

指令级 ISA 检查

CPU vs. ISA 指令模拟器

DiffTest-H: 低开销、高效率

3.2% 额外面积 @ Xilinx VU19P

定位 150+ Bugs @ 香山处理器

硬件加速的协同仿真

- 基于 **Emulator/FPGA:**
  - 硬件仿真器/FPGA: 仿真速度 1~100 MHz, **相较软仿最高加速 10,000 倍**
  - 软件参考模型:　　仿真速度约 100 MHz

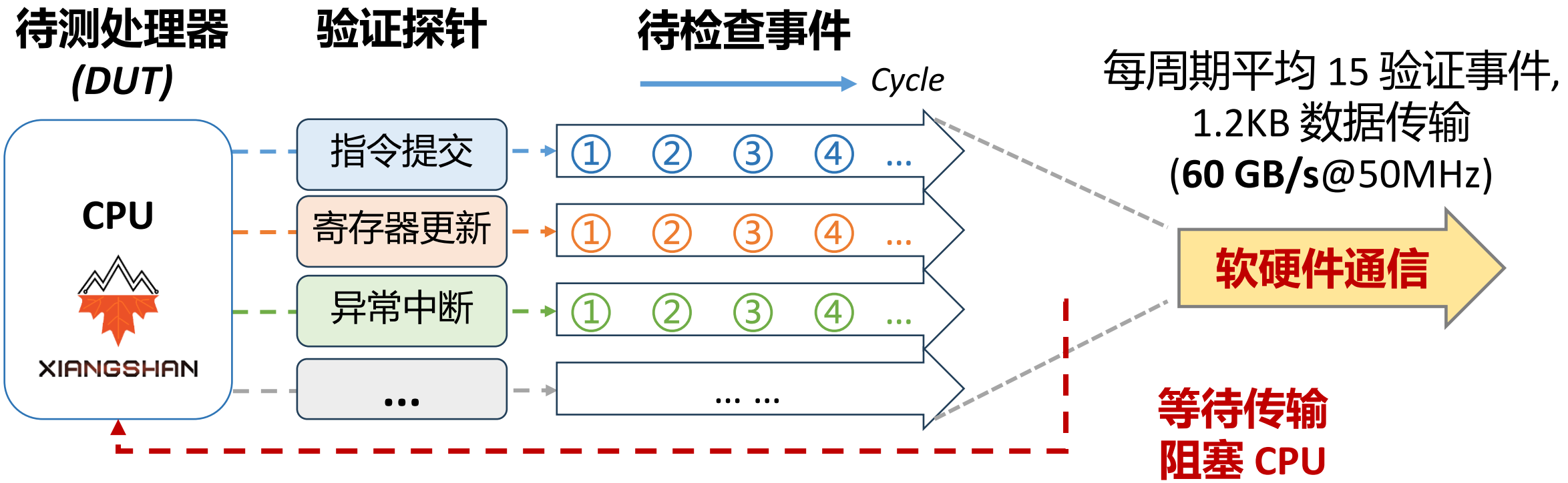


硬件加速的协同仿真

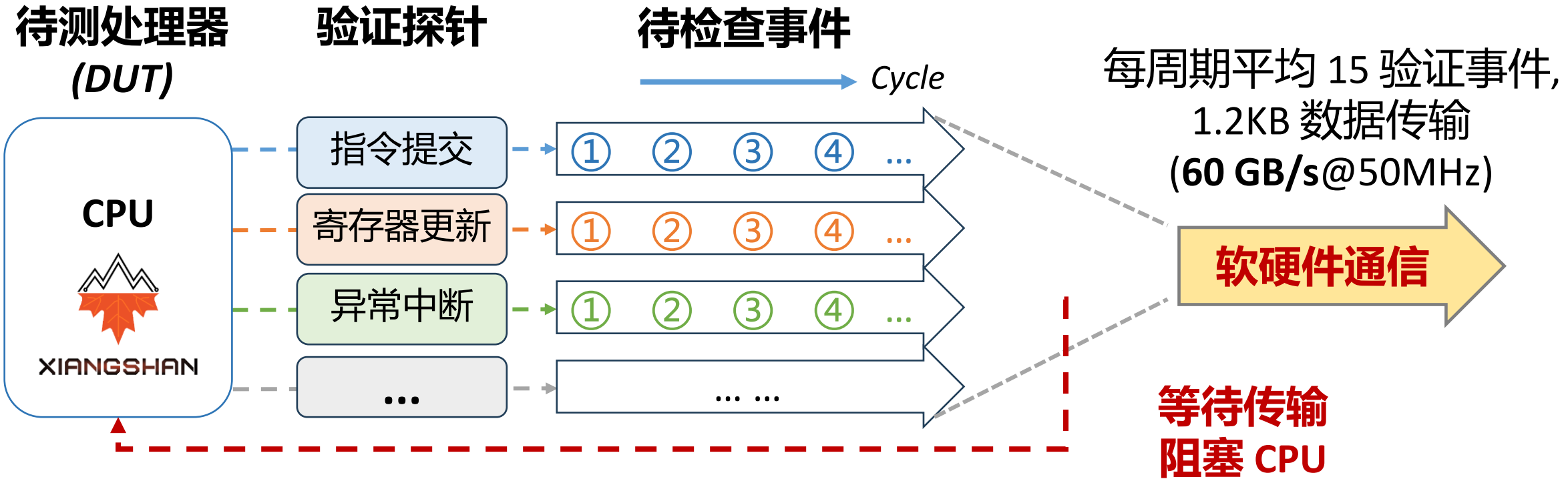
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软硬件通信在做什么?


待测处理器
(DUT)
验证探针
待检查事件
Cycle
CPU
XIANGSHAN
指令提交
寄存器更新
异常中断
...
① ② ③ ④ ...
① ② ③ ④ ...
① ② ③ ④ ...
... ...
每周期平均 15 验证事件,
1.2KB 数据传输
(60 GB/s@50MHz)
软硬件通信
等待传输
阻塞 CPU

软硬件通信在做什么?



通信优化?

- **事件聚合**: 分散验证事件 => 集中数据包, 易于传输及及解析
- **语义压缩**: 大量冗余数据 => 精简信息，减少 CPU 阻塞等待

事件聚合：紧凑拼接的统一格式数据包



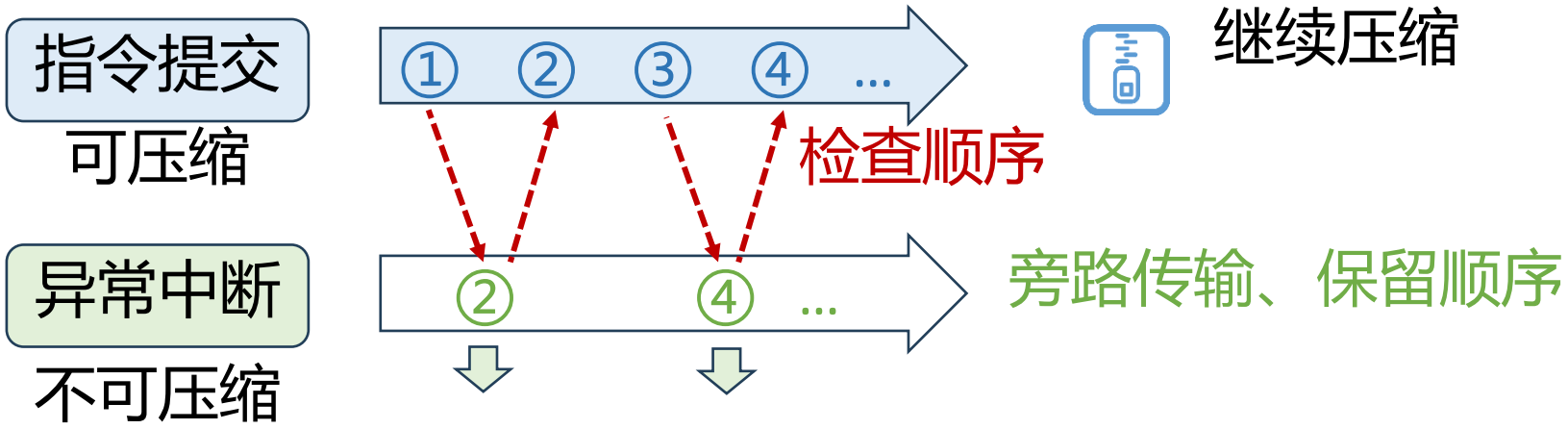
结构感知的打包策略

- 结构化元数据 (类别、大小)
- 硬件侧打包：并行偏移 & 拼接
- 软件侧解包：动态提取 & 解析

统一格式数据包

- 数据紧凑排列、减少冗余空泡
- 软硬件格式统一，便于解析
- 支持 PCIe/XDMA 等通用总线

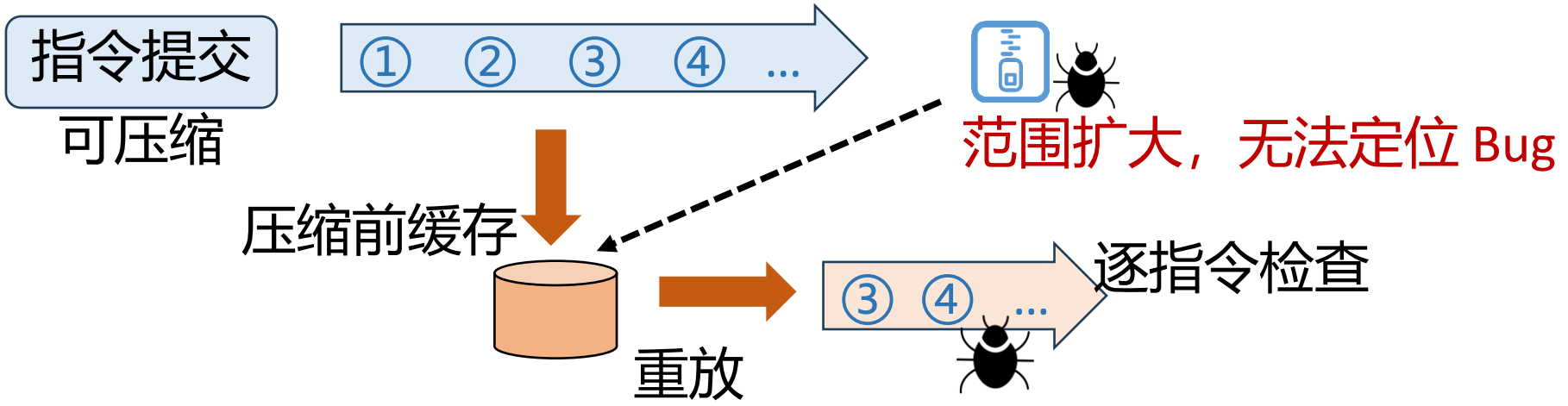
语义压缩: 顺序解耦的数据压缩方法



顺序解耦的压缩方法

- 验证事件遵循特定检查顺序
- 硬件侧调度：不可压缩事件旁路传输
- 软件侧重排：恢复检查顺序

语义压缩: 出错重放保留逐指令调试能力



顺序解耦的压缩方法

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- 软件侧重排：恢复检查顺序

出错重放，精确定位

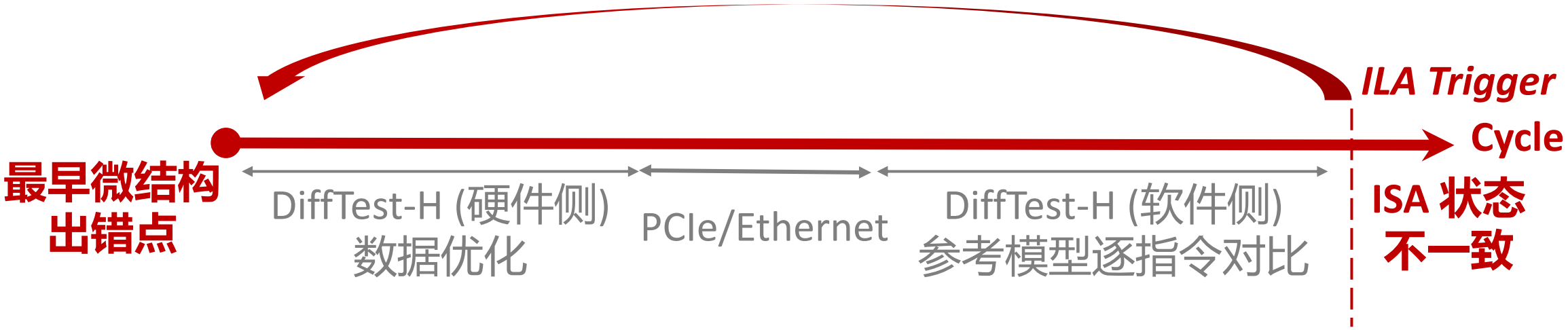
- 压缩扩大出错范围，难以定位 Bug
- 硬件侧缓存压缩前原始数据
- 软件侧通知重传，逐指令重新检查

调试: 指令级 ISA 状态检查 & 出错点最近波形

- **ISA 状态检查**: 指令级出错检查点 & 详细的 ISA 状态报告
  - 通常远早于串口状态观测（自检错误/结果错误/跑飞/卡死）
  - 更明确的调试入口（从出错指令/寄存器开始追踪原因）

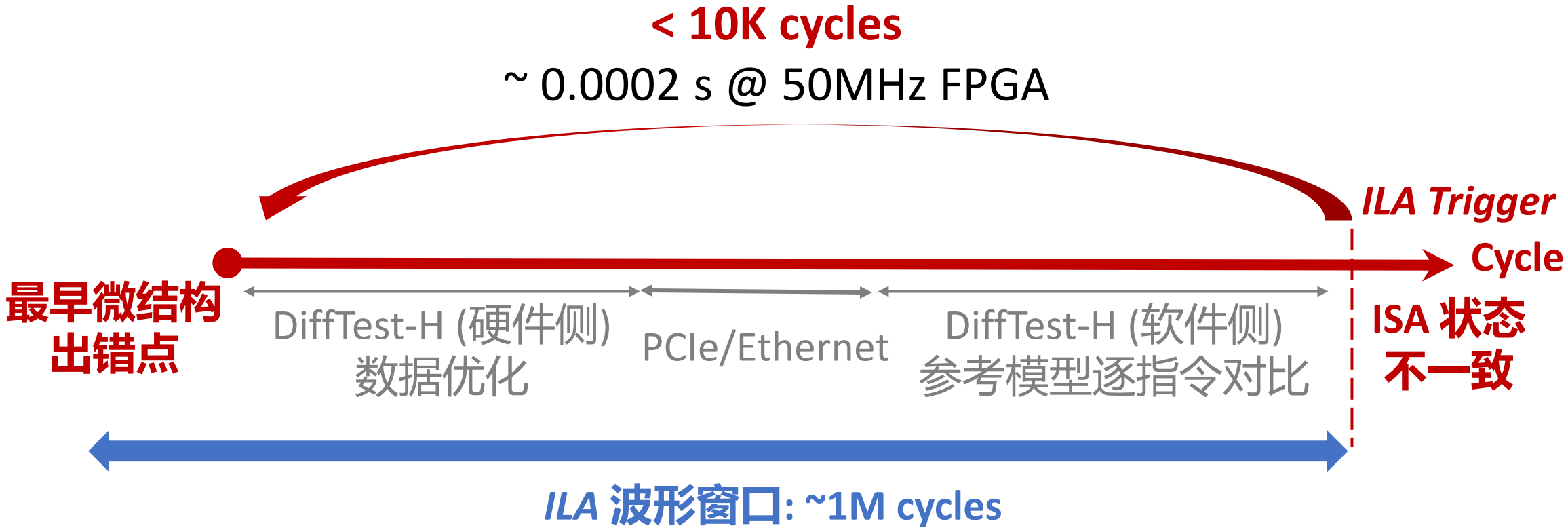
< 10K Cycles Gap

~ 0.0002 s @ 50MHz FPGA

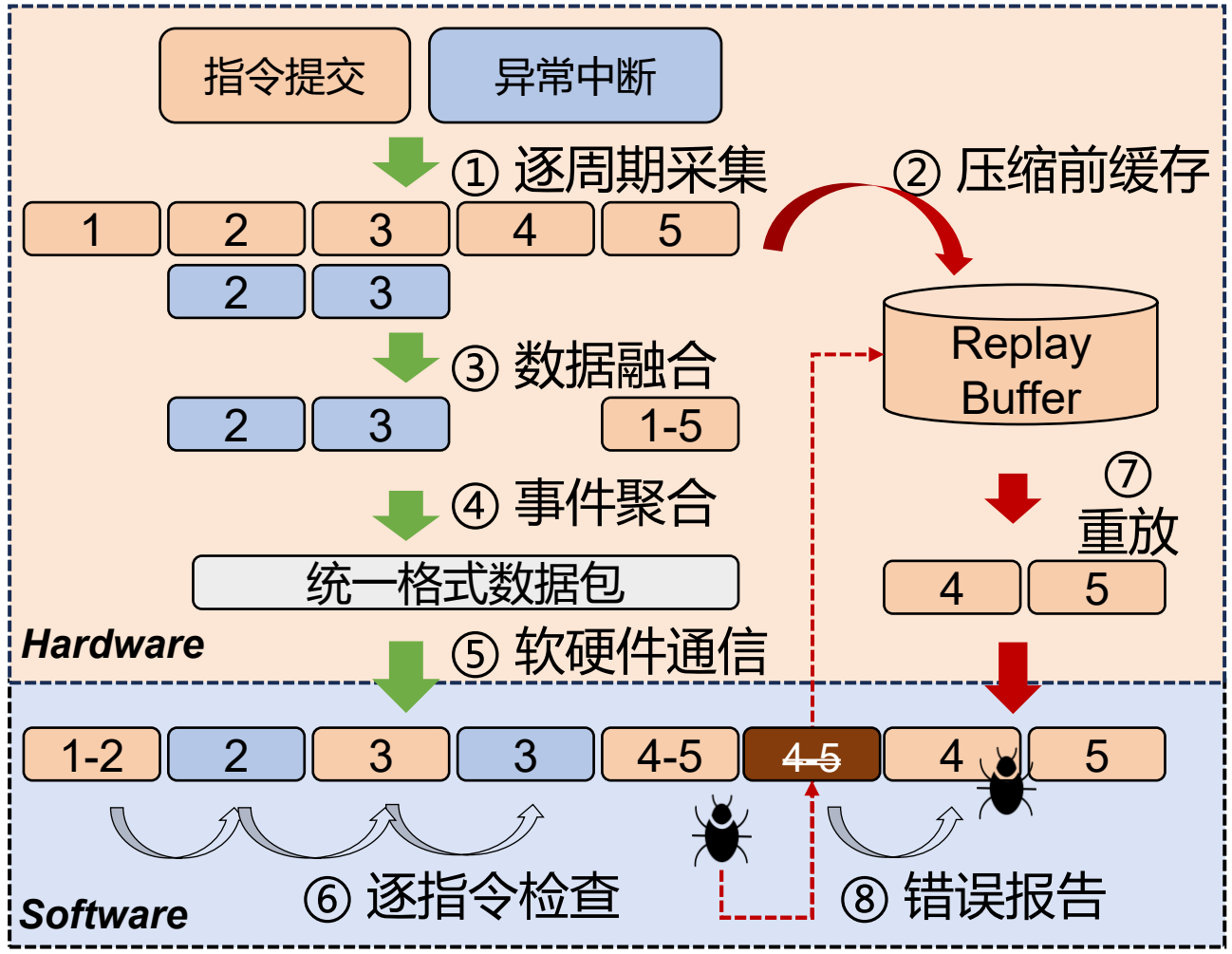


调试: 指令级 ISA 状态检查 & 出错点最近波形

- **ISA 状态检查**: 指令级出错检查点 & 详细的 ISA 状态报告
- **uArch 波形定位**: 自动设置 trigger，完整抓取出错点最近波形



DiffTest-H 工作流程



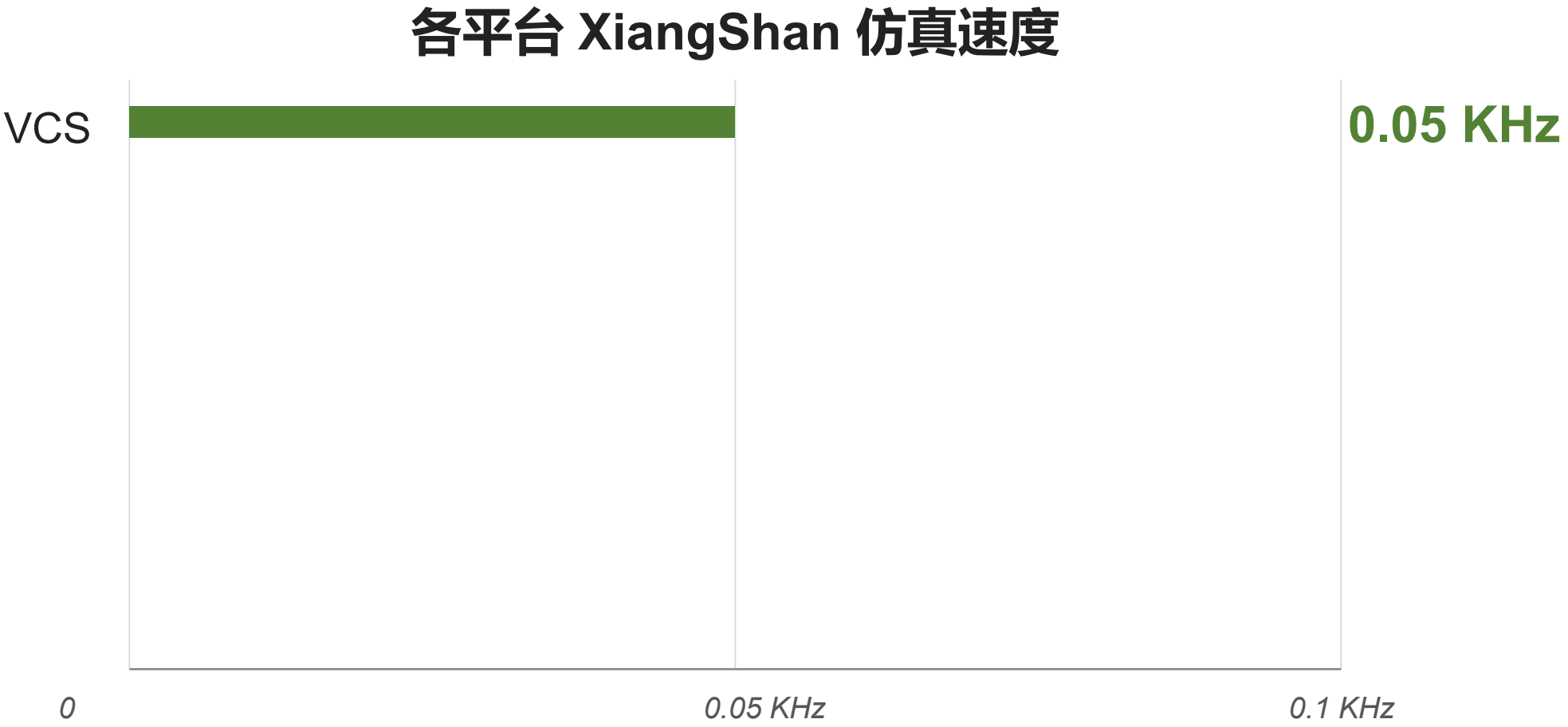
➡ 数据传输 & 优化 ➡ 出错调试

面积: 低开销的 FPGA 部署应用

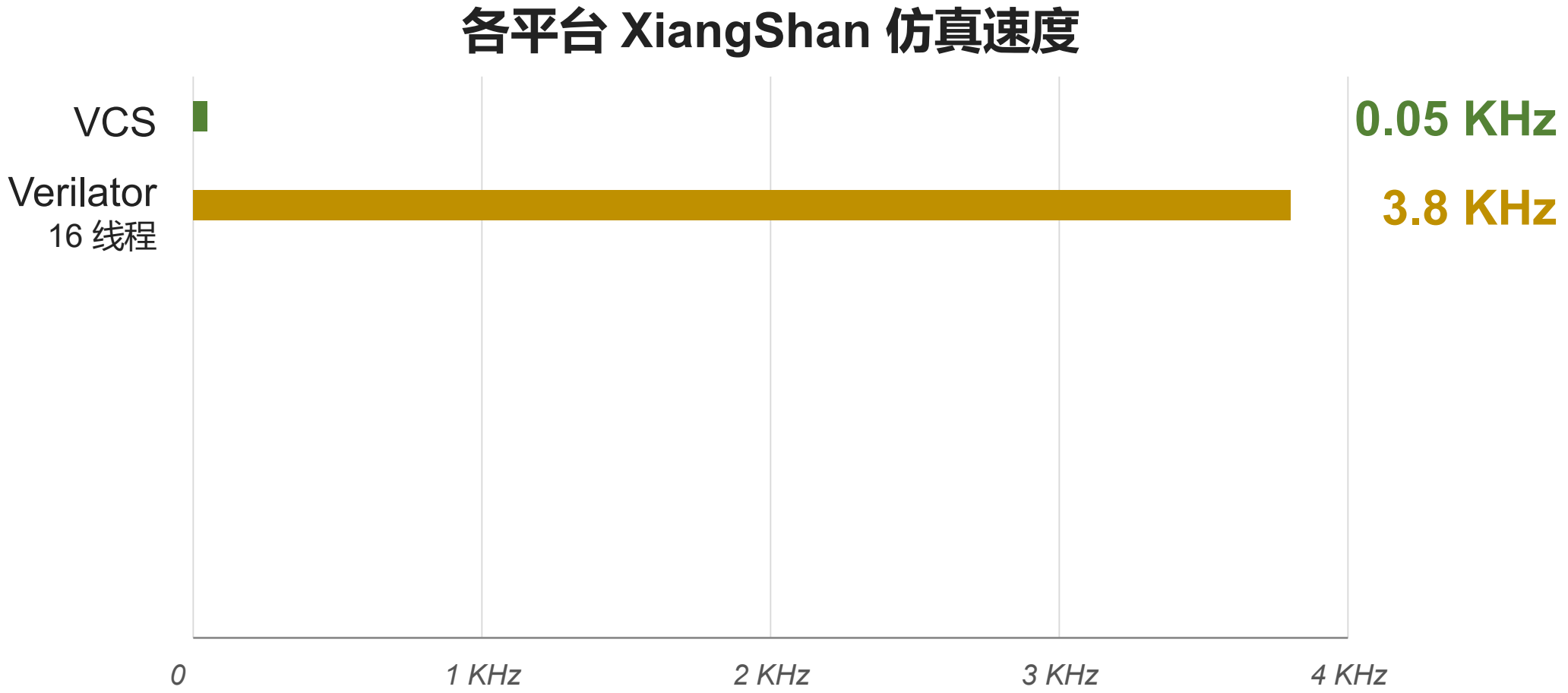
仅 **3% LUT** 开销 @ Xilinx VU19P
轻量便携，易于部署

	LUT	FF/Register	BRAM
XiangShan	59.6%	9.9%	24.3%
DiffTest-H	**3.3%**	**4.3%**	**0%**
Total	**62.9%**	**14.2%**	**24.3%**

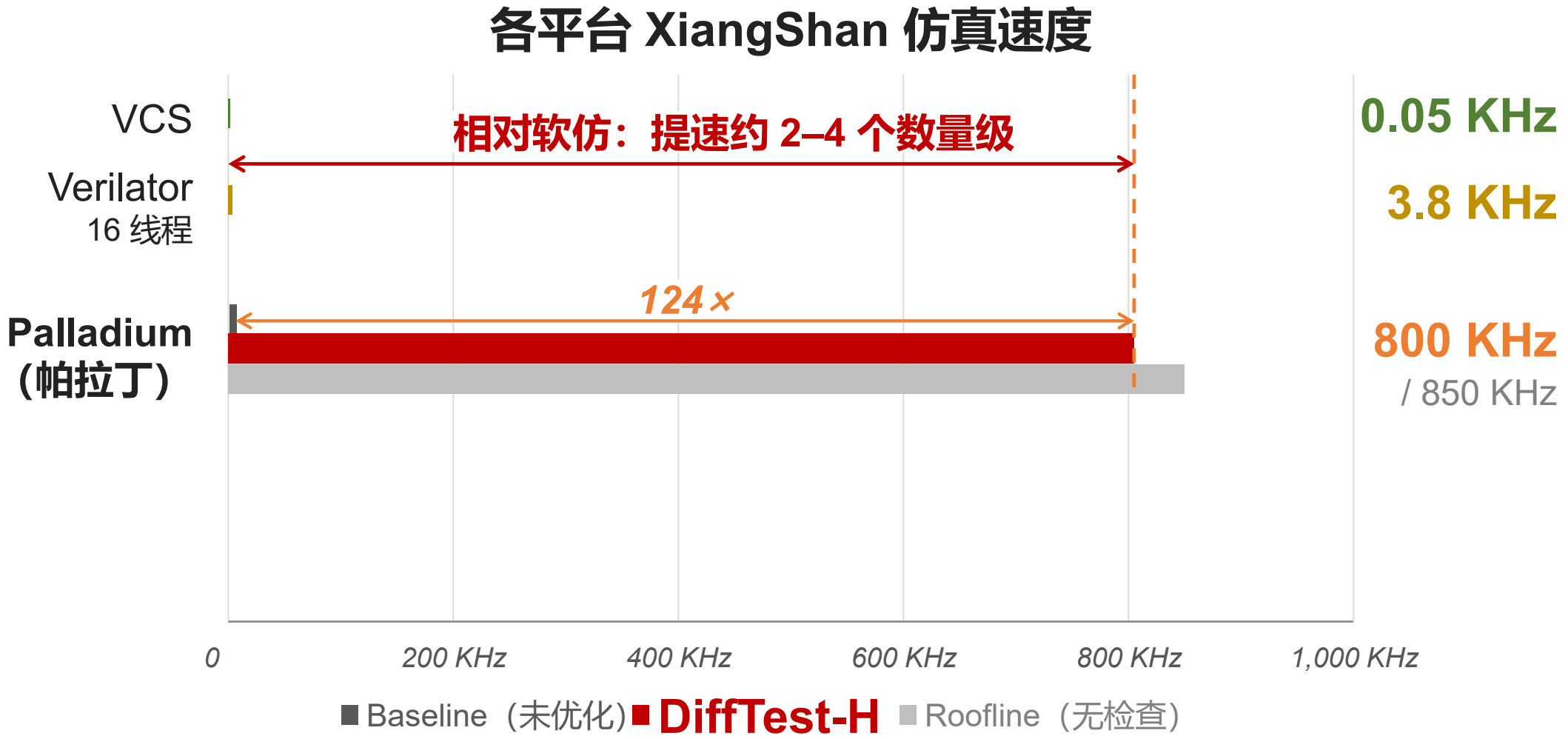
性能: 突破 30MHz 的高性能处理器验证



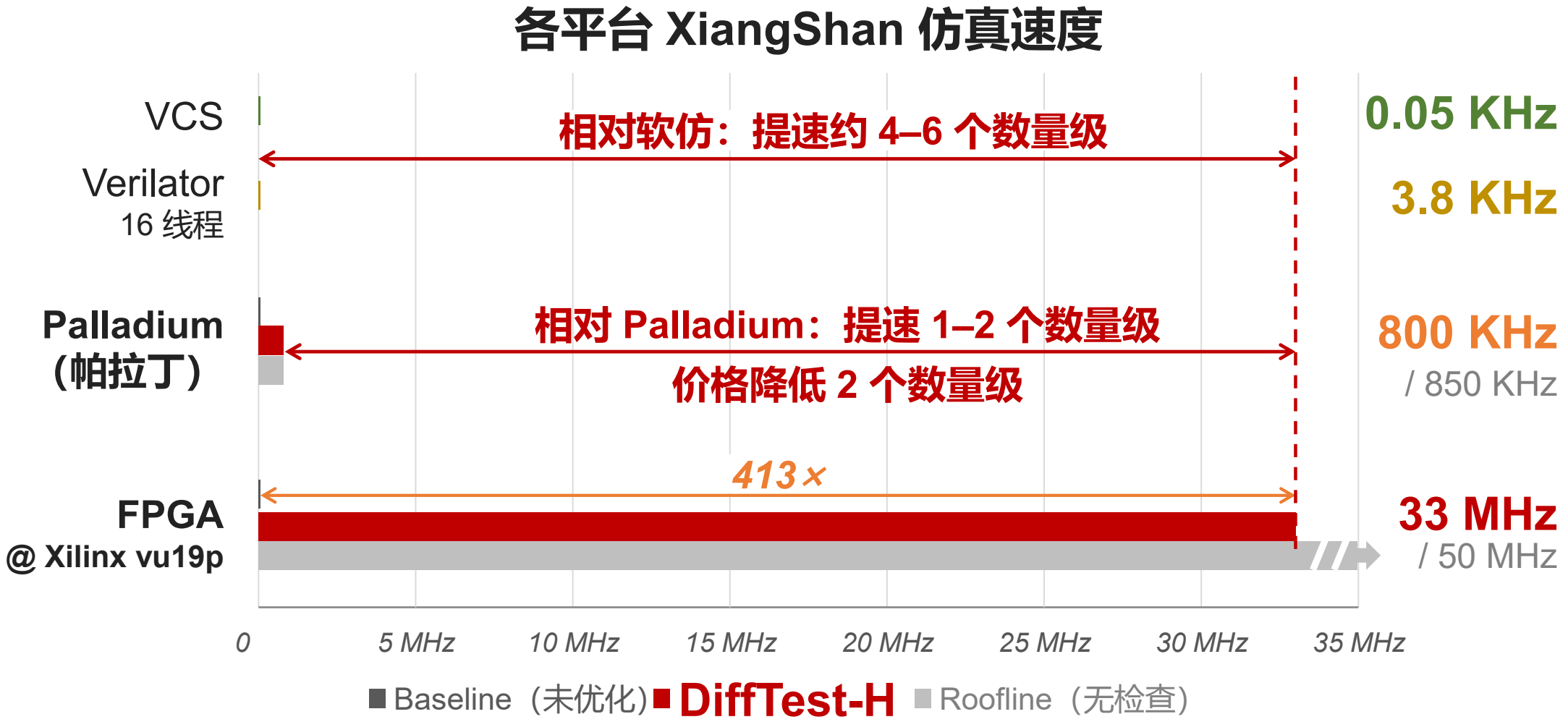
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性能: 突破 30MHz 的高性能处理器验证



性能: 突破 30MHz 的高性能处理器验证



DiffTest-H @ Xilinx vu19p：33 MHz

处理器缺陷发现：发现 150+ 香山处理器复杂Bug

- 六个月内，发现香山处理器 **150+ Bugs**
- 产生 19 个 PR，共计 780 + 行代码修改

fix(LoadUnit): fix misalign load wrong wakeup ✓
type: bug/confirmed
#4263 by cz4e was merged on Feb 16

fix(LSU): fix misalign store exception logic ✓
#4239 by Anzooooo was merged on Jan 26

fix(CSR): fix xTI[illegible] ✓
#4157 by sinceforYy [illegible] Jan 10

异常中断

fix(interrupt): `Vset` should not respond to interrupts ✓
#3991 by Anzooooo was merged on Dec 7, 2024

fix(VecExcp): isEnqExcp should be set 0 when writeback has older exception ✓
#3778 by huxuan0307 was merged on Oct 24, 2024

fix(exception): fix exception vaddr generate logic ✓
#3639 by good-circle was merged on Sep 27, 2024

fix(LoadUnit): uncache should not be generated when page fault ✓
#4442 by Anzooooo was merged on Mar 20

fix(StoreUnit): no uncache store misalign of mmio ✓
#4441 by Anzooooo was merged on Mar 20

fix(StoreQueue): fix the `vecExceptionFlag` setting condition ✓
#4037 by [illegible]

缓存一致性

fix(TLB): avoid freeze when GPF occurs ✓
#3964 by cebarobot was merged on Dec 2, 2024

fix(ICache): block waylookup if there is a pending gpf ✓
#3719 by ngc7331 was merged on Oct 12, 2024

fix(TLB, RVH): delete the s1tagfix which maybe cause the tag check to fail ✓
#3685 by pxk27 was merged on Sep 30, 2024

submodule(CoupledL2): bump CoupledL2 ✓
#3621 by linjuanZ was merged on Sep 21, 2024

fix(vector): do not set vs.dirty for some type of vecInsts ✓
#3965 by Tang-Haojin was merged on Dec 1, 2024

fix(vstart): fix vstart wrong update when other instruction handling interrupt ✓
#3887 by Tang-Haojin was merged on Nov 18, 2024

fix(vstart): fix vstart wrong update when other instruction handling ✓
#3870

向量控制逻辑

feat(rv64v): fix exception for vector fof/non-fof load ✓
#3695 by huxuan0307 was merged on Oct 4, 2024

feat(rv64v): Added support for vector's vstart, first-only-fault, trigger ✓

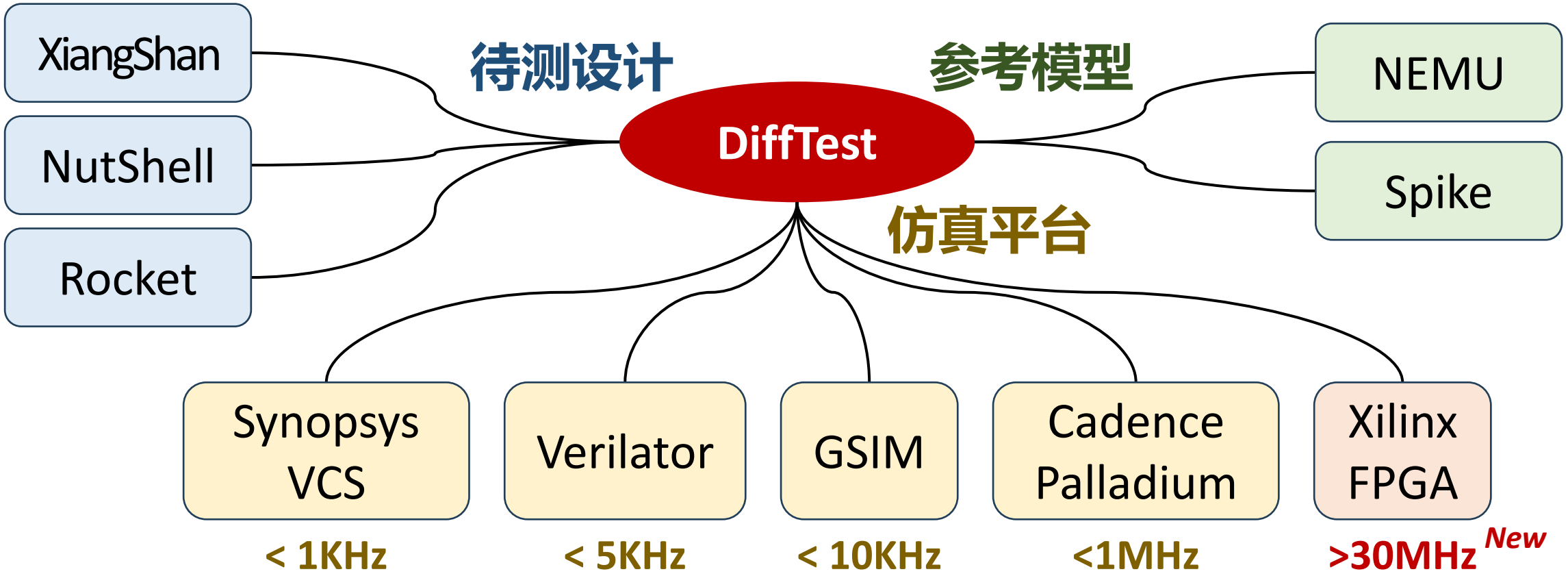
feat(Difftest): add multi-core vector load check ✓
#4361 by Anzooooo was merged on Mar 7

fix(vtypegen): fix initial condition after receive redirect ✓
#3664 by Ziyue-Zhang was merged on Sep 27, 2024

fix(VLSU): fix bug in flush of pipeline connect & skid buffer ✓
#3646 by weidingliu was merged on Sep 26, 2024

DiffTest: 开源开放的协同仿真框架

- https://github.com/OpenXiangShan/difftest



DiffTest-H: 突破 30 MHz 的高性能处理器验证框架

- **DiffTest-H:** 硬件平台加速的处理器核协同仿真验证框架
  - **完整香山昆明湖，完整 RVA23** 验证支持
  - **指令级 ISA 验证**，波形能力增强
  - **>30 MHz 仿真速度**@Xilinx VU19P, **3% 面积开销**
  - 落地香山处理器, 发现 **150+** 功能缺陷
  - **开源开放** @github/OpenXiangShan/difftest
  - **论文发表于** MICRO 2025

XIANGSHAN

GitHub 项目
DiffTest-H

论文
MICRO'25

- **欢迎 CPU IP / EDA 公司商业 & 技术合作**
  - **合作联系方式**: xuyinan@ict.ac.cn

感谢聆听！