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Functional Verification for Agile Processor Development: A Case for Workflow Integration


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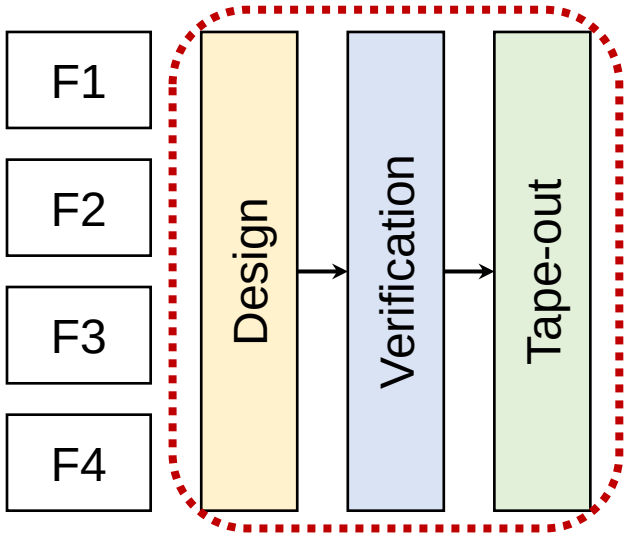
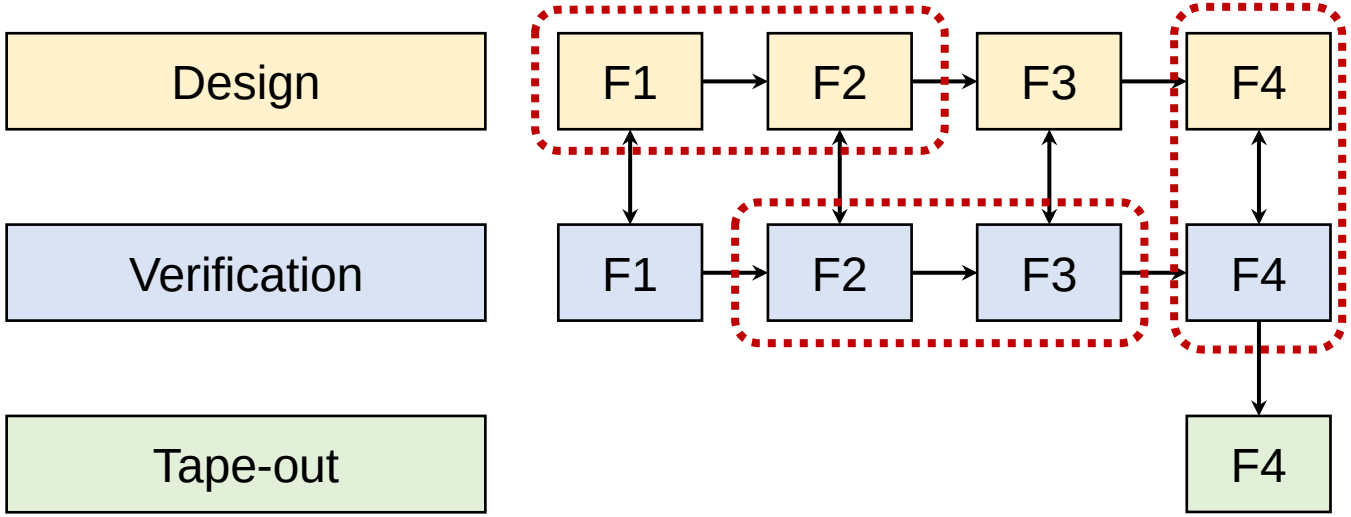
The Era of Agile Processor Development



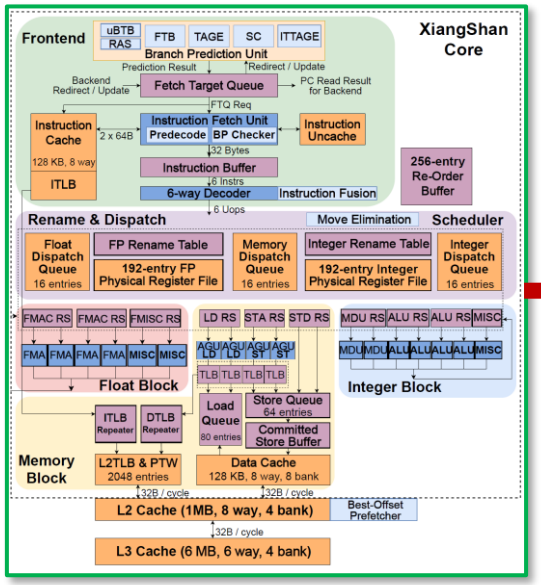
Waterfall Model



Agile Model

Dynamic Functional Verification

Design Under Test (DUT)



Spike RISC-V ISA Simulator

NEMU

imperas OVP Open Virtual Platforms

QEMU

RISCV Sail Model

Dromajo

Reference Model (REF)

eembc/coremark
OSCPU/nexus-am
SPEC CPU® 2006
riscv-non-isa/riscv-arch-test
chipsalliance/riscv-dv

Test Generation

Co-Simulation

Mismatch

Fault Analysis

GTKWave
Synopsys DVE/Verdi

Dynamic Functional Verification with *Agile Development*

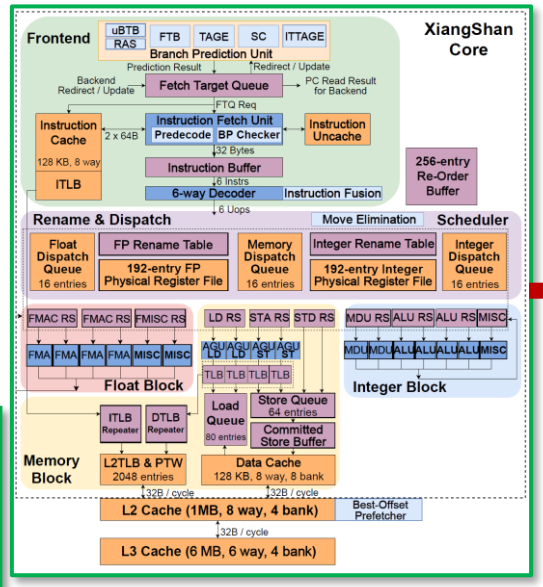
CHISEL

Design Under Test (DUT)

Rocket Chip Generator

NutShell (果壳)

XiangShan (香山)



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Test Generation

???

Co-Simulation

???

Mismatch

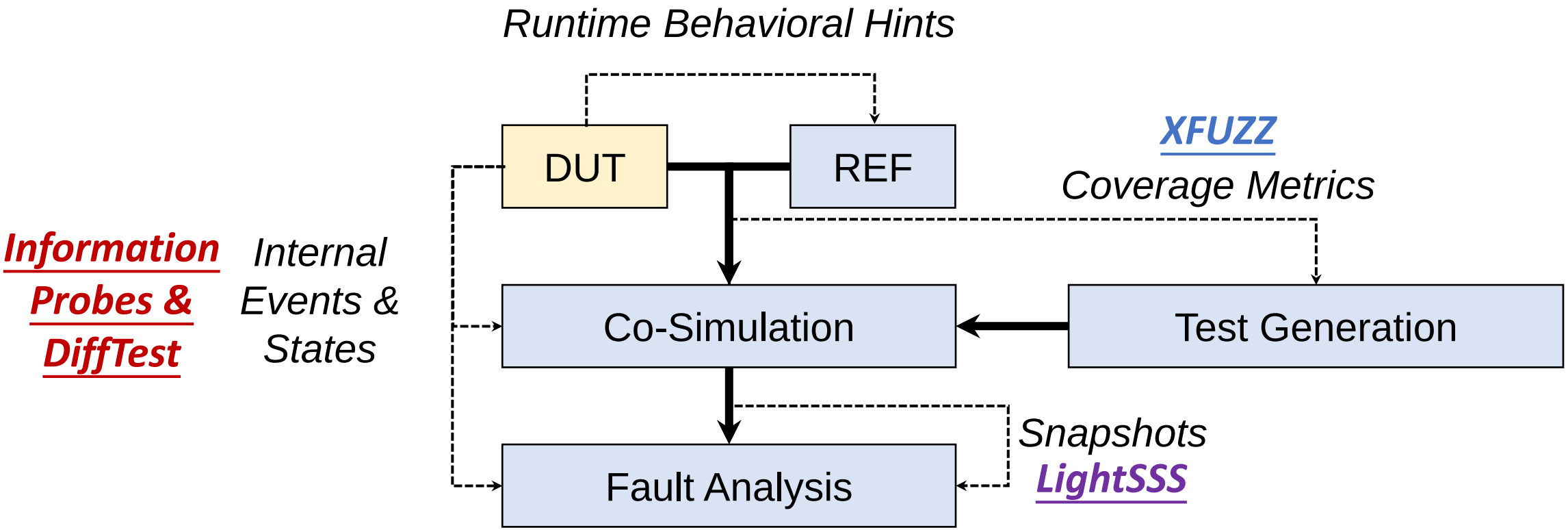
GTKWave
Synopsys DVE/Verdi

Fault Analysis

???

Proposed Methods and Tools

Diff-Rule Based Agile Verification (DRAV)



Verifying RISC-V Processors

RISC-V CPU

Rocket Chip Generator

NutShell (果壳)

XiangShan (香山)

- ArchEvent
- InstrCommitEvent
- TrapEvent
- CSRState
- DebugModeState
- ArchIntRegState
- ArchFpRegState
- ArchIntDelayedUpdate
- ArchFpDelayedUpdate
- IntWritebackEvent
- FpWritebackEvent
- StoreEvent
- SbufferEvent
- LoadEvent
- AtomicEvent
- RefillEvent
- LrScEvent

Information Probes

RISC-V REF

Spike

NEMU

- memcpy
- regcpy
- exec
- guided_exec
- raise_intr
- debug_mem_sync
- store_commit
- csrcpy
- uarch_sync
- update_config
- load_flash_bin
- set_ramsize
- disambiguation_state

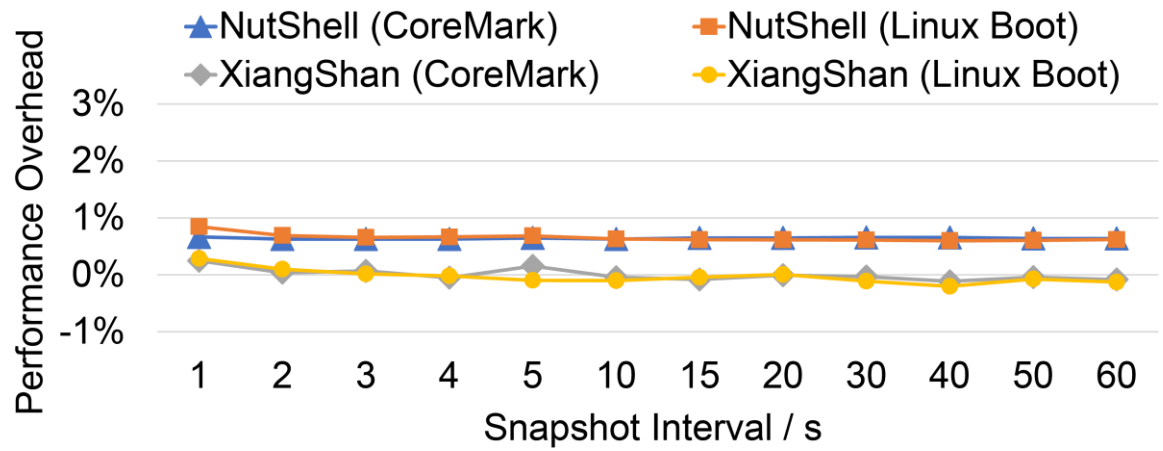
REF Proxy Interfaces

Co-Simulation

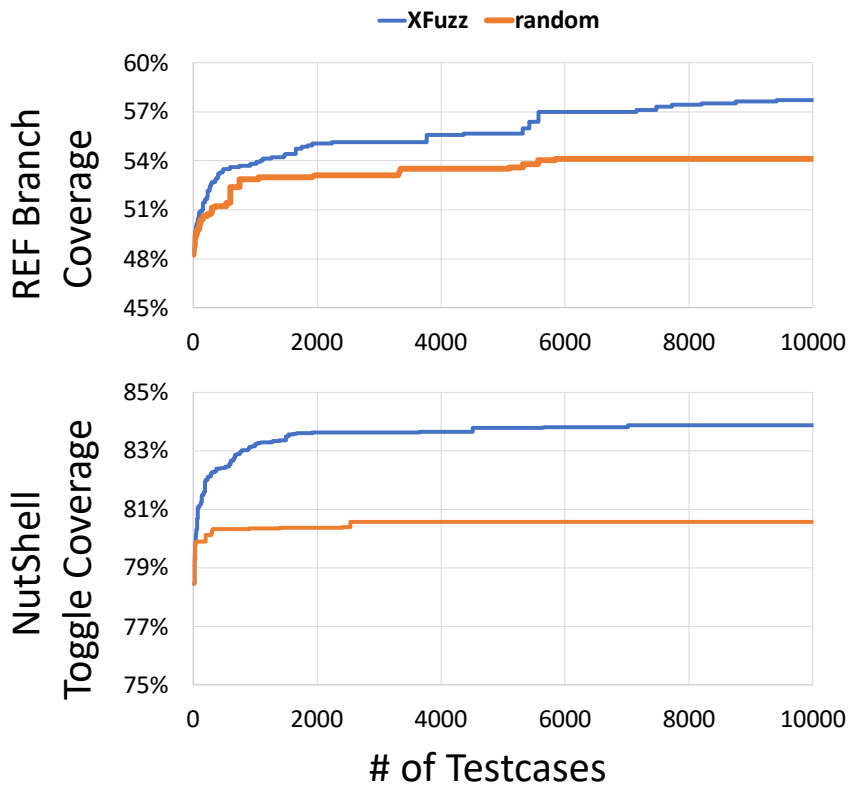
Verifying RISC-V Processors – Cont.

33 Functional Bugs Found in NutShell

Category	Bug ID	Descriptions
Arithmetic	769669f	32-bit AMO instructions do not sign-extend the 32-bit operands.
CSR Operations	42c8460	Reserved and non-writable fields in `mstatus` may be written by CSR instructions.
	ef78025	The virtual address is not zero-extended to 64-bit if virtual memory is disabled.
	5b60e9c	`mtval/stval` is incorrectly updated without considering the exception delegation.
	b86c319	`mstatus.mprv` is not cleared when `MRET/SRET` to a mode less privileged than `M`.
	6f4cd05	`mstatus.mpp` is updated and read with an illegal value (`ModeH`).
Access Control	54367ce	An illegal jump target causes mistakenly executed load/store operations.
	f23acbf	Misaligned `LR/SC` operations are not detected as address-misaligned exceptions.
	5dd6a74	Non-existent CSRs such as `pmpcfg1` and `pmpcfg3` are enabled in RV64.
	ccd9c7f	`CSRRC/CSRRCI` causes write side effects when `rs1=x0` or `uimm[4:0]=0`.
	7f928a3	`SC` incorrectly updates the reservation sets that should be set by `LR` only.
	f8acb2a	`mstatus.TVM` does not intercept supervisor virtual-memory management operations.
	c508b32	Large pages with misaligned PPNs are not detected as page-fault exceptions.

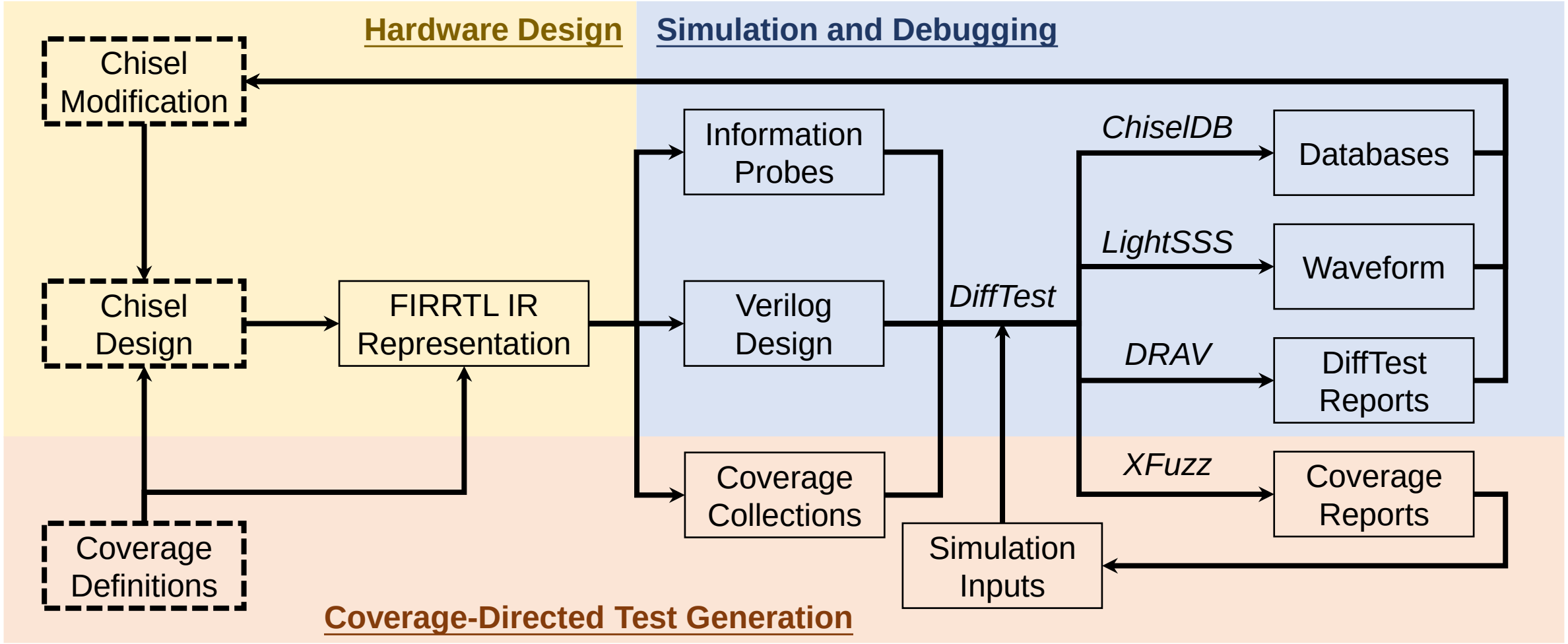


Higher Coverage for NutShell and REF



<1% Performance Overhead for Snapshots
An Order of Magnitude Lower than SOTA

How? Workflow Integration!



Key Principles: Collaborative Task Delegation + Dynamic Information Exchange

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A Paper from the XiangShan Team

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